REMARKS

Claims 4-5, 7-9, 13, 21, 42, 44-45, 48, 51, 68, 83-84, and 88 have been amended. Claims 6, 47, and 87 have been canceled. No new claims have been added. Claims 1-5, 7-86 and 88 are pending.

Claims 4-5, 7-8, 13-14, and 44-45 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 4-5, 7-8, 13, and 44-45 have been amended to address the rejection. Claims 4-5, 7-8, 13-14, and 44-45 are now believed to be in full compliance with 35 U.S.C. § 112, second paragraph. Accordingly, the rejection to claims 4-5, 7-8, 13-14, and 44-45 under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claims 1-3, 6-11, 21-24, and 33-34 stand rejected as being anticipated by Perino (U.S. Patent No. 6,426,984). Claims 84-85 stand rejected as being anticipated by Yamagishi (U.S. Patent No. 6,366,190). Claims 12 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino and Yamagishi. Claims 15-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino and Magro (U.S. Patent No. 6,516,362). Claims 30-32 and 35-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, Yamagishi, and Magro. Claim 37 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino, Yamagishi, Magro, and Mizukami (U.S. Patent No. 5,422,858). Claims 38-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino and Gillingham (U.S. Patent No. 6,510,503). Claims 25-28 and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino and Gasbarro (U.S. Patent No. 5,432,823). Claims 68-69, 72-73, and 78-83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino, Gasbarro, and Gillingham. Claim 74 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino, Gasbarro, Gillingham, and Yamagishi. Claims 43-67 and 75-77 stand rejected under Perino, Gasbarro, Gillingham, and Magro. Claim 86 stands rejected under 35 U.S.C. §

103(a) as being unpatentable over Yamagishi and Mizukami. Claim 88 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Gasbarro and Magro. These rejections are respectfully traversed.

Claims 1, 42 recite, *inter alia*, "wherein said first and second clock signals are independent signals, one of said first and second clock signals is a data write clock signal, and the other of said first and second clock signals is a data read clock signal."

Claim 68, 83-84, and 88 recite, *inter alia*, "wherein said data write clock signal and said data read clock signal are independent signals."

Perino discloses a memory system 70 which features two clock domains. As shown in Fig. 5, one clock domain comprise the CLOCK1 signal and another clock domain comprise the CLOCK2 signal. The CLOCK1 and CLOCK2 signals are independent signals generated by the clock generator 72. The CLOCK1 signal propagates along a looping path from the clock generator 72 through devices 26A ... 26N and terminates at a memory controller 24. The CLOCK2 signal propagates from the clock generator 72 to a pad 78 of the memory controller and then propagates through devices 26A ... 26N before terminating at termination block 31. A clock latency adjustment circuit 74 monitors the phase relationship between CLOCK1 and CLOCK2 at nodes A and B, respectively and maintains a predetermined phase relationship between the two clock domains at nodes A and B. Significantly, Perino does not teach or suggest that one clock domain corresponds to a read clock, i.e., a clock governing read operations, while another clock domain corresponds to a write clock, i.e., a clock governing write operations. The Office Action asserts that Fig. 5 discloses the use of a read clock and a write clock, however, all Fig. 5 shows is that there are two clock domains in the memory system 70. Accordingly, Perino fails to disclose or suggest the above quoted limitations of claims 1, 42, 68, 83-84, and 88.

Yamagishi discloses a high speed synchronous memory device. Referring to Fig. 1, it can be seen that the memory device 1 accepts a basic clock signal which drives a PLL 3. The PLL 3 outputs a signal to a clock generator 4 which generates a plurality of internal clock signals. Each internal clock signal is routed into a respective storage element group 5a ... 5n, and drives a respective PLL 51a ... 51n. The PLL regenerates the clock signal and distributes it to individual storage elements. One of the storage elements 5n also routes the output of its PLL 51n to a PLL which regenerates the signal as a return clock signal to a clock tree circuit 7. Yamagishi therefore does not disclose or suggest the use of read and write clock signals. Additionally, since each of the clock signals in the storage apparatus 1 is a PLL synchronized version of the basic clock signal, none of the clock signals can be said to be an independent signal. Accordingly, Yamagishi fails to disclose or suggest the above quoted limitations of claims 1, 42, 68, 83-84, and 88.

Gasbarro discloses at Fig. 3 a memory system where a clock signal is propagated in a loop so that the clock signal travels along both a receive direction and a transmit direction. When the same clock signal is traveling in one direction, it can be used as a read clock signal, but when the clock signal loops back in the opposite direction, it can be used as a write clock signal. Gillingham similarly discloses a high bandwidth memory interface utilizing clock generators which generate a single clock which propagates along a looped path. Accordingly, the clock signals of Gasbarro and Gillingham are not independent read and write clock signals. Accordingly, Gasbarro and Gillingham fail to teach or suggest the above quoted limitations of claims 1, 42, 68, 83-84, and 88.

The Office Action further cites to Mizukami and Magro. However, these references also fail to disclose or suggest the above quoted limitations of the independent claims.

Accordingly, claims 1, 42, 68, 83-84, and 88 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2-5, 7-41, 43-46, 48-67, 69-82, and 85-86) are also believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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